UNITED STATES PATENT AND TRADEMARK OFFICE

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10/692,683	10/27/2003	Chia-Hsin Chen	2450-0577P	2047

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EXAMINER
HSU, JONI

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/692,683	CHEN, CHIA-HSIN
	Examiner	**Art Unit**	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☒ Claim(s) *1 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____ .

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ .

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

Claim Objections

1.   Claim 1 is objected to because of the following informalities: Claim 1 recites "input processing" where it should recite "input processing *unit*", "output processing" where it should recite "output processing *unit*", and "plurality of First-In-First-Out (FIFO) sub unit" where it should recite "plurality of First-In-First-Out (FIFO) sub units". Also, "step(5)" is misspelled. Appropriate correction is required.

2.   Claim 5 is objected to because of the following informalities: Claim 5 recites "FIFO unit has said memory depth *is* equal to" where it should recite "FIFO unit has said memory depth equal to". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.   Claims 1, 4, and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitations "the memory architecture", "the using of access frequency

and memory depth", "said first access frequency", and "said readout". There is insufficient

antecedent basis for these limitations in the claim.

Claim 4 recites the limitation "the same access frequency". There is insufficient

antecedent basis for this limitation in the claim.

Claim 6 recites the limitations "said queue" and "the deferent frequency". There is

insufficient antecedent basis for these limitations in the claim.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or
> described as set forth in section 102 of this title, if the differences between the subject
> matter sought to be patented and the prior art are such that the subject matter as a whole
> would have been obvious at the time the invention was made to a person having ordinary
> skill in the art to which said subject matter pertains. Patentability shall not be negatived
> by the manner in which the invention was made.

6.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness
        or nonobviousness.

7.   Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marlton

(US005594467A), in view of Min (US006184907B1), further in view of Yamada

(US006333788B1).

8.   With regard to Claim 1, Marlton describes a method for an image reducing processing

circuit (Col. 7, lines 33-35, 42-45; Col. 8, lines 9-11, 47-49, 56-59; Col. 25, lines 7-9) including

the memory architecture of two First-In-First-Out (FIFO) units (500, Figure 5; 224, Figure 13)

for simplifying the using of access frequency and memory depth, the method comprising the

following steps of: (1) providing an input processing unit (26, Figure 2; Figure 3) receiving

input image data and delivering the image data (88) (Col. 5, lines 42-48); (2) providing a

horizontal direction image processing (100, 104, 106, Figure 4) receiving the image data from

step(1), quantifying the image data in the horizontal direction (Col. 7, lines 14-64); (3) providing

a first step First-In-First-Out (FIFO) (110, Figure 4; 32, Figure 11; 500, Figure 5) receiving the

image data from step(2) to read and write the image data, and having a plurality of First-In-First-

Out (FIFO) sub units receiving and delivering the image data in sequence (Col. 7, line 65-Col. 8,

line 3; Col. 9, lines 56-61; Col. 10, lines 6-14); (4) providing a vertical direction image

processing (116, Figure 4) receiving the image data from step(3) (Col. 8, lines 29-32), reading

and writing completely the image data, quantifying the image data in the vertical direction (Col.

8, line 33-Col. 9, line 55); (5) providing a second step First-In-First-Out (FIFO) (34, Figure 2;

224, Figure 13; Col. 4, lines 44-45) receiving the image data from step(4) (Col. 5, lines 56-59),

and having a First-In-First-Out (FIFO) memory element implementing the readout and writing of

the image data (Col. 14, lines 51-52; Col. 14, line 63-Col. 15, line 28); and (6) providing an

output processing unit (34, Figure 2), receiving the image data from step(5), and outputting

reduced image data (Col. 4, lines 44-45; Col. 5, lines 65-67; Col. 26, lines 20-24).

However, Marlton does not specifically teach that the first step FIFO reads and writes

image data with a first access frequency, the second step FIFO implements the readout and

writing of the image data on the first access frequency and a second access frequency, and the

output processing unit works on the second access frequency. However, Min describes that the

access frequency is determined by the FIFO capacity (Col. 1, lines 62-63). Marlton describes

that the first step FIFO (550, Figure 5) has a capacity of 256Kx4 (Col. 10, lines 6-8) and the

second step FIFO (224, Figure 13) has a capacity of 1 Mbit (Col. 14, lines 51-52). Therefore,

Marlton inherently discloses that the first step FIFO reads and writes image data with a first

access frequency. Since the second step FIFO is receiving data that was in the first step FIFO

and the FIFOs have different capacities, the second step FIFO must inherently implement the

readout and the writing of the image data on the first access frequency and a second access

frequency. Since the output processing unit (34, Figure 2) receives image data from the second

step FIFO, the output processing unit inherently works on the second access frequency.

It would have been obvious to one of ordinary skill in this art at the time of invention by

applicant to modify the device of Marlton so that the first step FIFO reads and writes image data

with a first access frequency, the second step FIFO implements the readout and writing of the

image data on the first access frequency and a second access frequency, and the output

processing unit works on the second access frequency as suggested by Min because Min

suggested that the access frequency is determined by the FIFO capacity (Col. 1, lines 62-63),

which is well-known in the art, and Marlton describes that the FIFOs have different capacities

(Col. 10, lines 6-8; Col. 14, lines 51-52).

However, Marlton and Min do not specifically teach that the horizontal direction image

processing transfers the image data to column signals with a row column type and the vertical

direction image processing transfers the image data to row signals with a row column type.

However, Marlton described that the horizontal direction image processing is a horizontal

interpolator (104, 106, Figure 4) and the vertical direction image processing is a vertical

interpolator (120, 121). Yamada describes that horizontal interpolation processes the image data

in columns (Col. 13, lines 42-55), and therefore inherently transfers the image data to column

signals with a row column type, and vertical interpolation processes the image data in rows (Col.

13, lines 26-41), and therefore inherently transfers the image data to row signals with a row

column type.

It would have been obvious to one of ordinary skill in this art at the time of invention by

applicant to modify the devices of Marlton and Min so that the horizontal direction image

processing transfers the image data to column signals with a row column type and the vertical

direction image processing transfers the image data to row signals with a row column type as

suggested by Yamada because Marlton describes horizontal and vertical interpolators (104, 106,

120, 121), and Yamada describes that this is how horizontal and vertical interpolation is

performed (Col. 13, lines 42-55; Col. 13, lines 26-41), which widely used and well-known in the

art.

9. With regard to Claim 2, Marlton describes that the input image data received by the input processing unit (26, Figure 2; Figure 3) is image data from a video source (28, Figure 2; Col. 5, lines 42-46), so this image data is inherently original image data.

10. With regard to Claim 3, Marlton describes that the output processing unit (34, Figure 2) is a medium means for outputting image data (Col. 5, lines 65-67).

11. Claims 4, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marlton (US005594467A), in view of Min (US006184907B1), further in view of Yamada (US006333788B1), further in view of Kemeny (US006701393B1).

12. With regard to Claim 4, Marlton, Min, and Yamada are relied upon for the teachings as discussed above relative to Claim 1. Marlton describes that providing a first step First-In-First-Out (FIFO) unit (110, Figure 4; 32, Figure 11; 500, Figure 5). Marlton describes that the first step FIFO receives the image data from the horizontal interpolator (106, Figure 4; Col. 7, line 65-Col. 8, line 3; Col. 9, lines 56-61; Col. 10, lines 6-14), and the video input lines to the first step FIFO are horizontal lines (130, Figure 6, Figure 7). These lines are then fed to the vertical scaler (116, Figure 4; Col. 9, lines 23-26). Therefore, Marlton inherently discloses that receiving the image data and delivering the image data in sequence includes the following steps: (1) reading the image data in the horizontal direction, and writing the image data on a first access frequency by using a First-In-First-Out (FIFO) way; and (2) outputting the image data in the

horizontal direction in sequence on the first access frequency; and (3) when running step(1) and step(2), both of them are working at the same frequency (Col. 10, lines 6-20).

However, Marlton, Min, and Yamada do not teach writing the image data into a queue. However, Kemeny describes a first (42-0, Figure 3) and second (42-1) FIFO queue with different access frequencies. The first FIFO queue writes and outputs data at the same frequency (Col. 10, line 59-Col. 11, line 7).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Marlton, Min, and Yamada to include writing the image data into a queue as suggested by Kemeny because Kemeny suggests that the advantage of using FIFO queues is that data can be ordered according to priority (Col. 1, line 60-Col. 2, line 4).

13.   With regard to Claim 6, Marlton describes that providing the second step First-In-First-Out (FIFO) (34, Figure 2; 224, Figure 13; Col. 4, lines 44-45). Marlton describes that the second step FIFO receives the image data from the vertical interpolator (116, Figure 4; Col. 8, line 33-Col. 9, line 55; Col. 5, lines 56-59). Therefore, Marlton inherently discloses that receiving the image data and transferring image data includes the following steps: (1) reading the image data in the vertical direction; and (2) outputting the image data in the vertical direction in sequence (Col. 14, lines 66-67). As discussed in the rejection for Claim 1, the second step FIFO receives data that was in the first step FIFO, and the FIFOs have different capacities, so the second step FIFO must inherently read and write the image data on the first access frequency by using the First-In-First-Out (FIFO) way; and output the image data on the second access frequency; and when running step(1) and step(2), both of them are working at the deferent frequency.

However Marlton does not teach writing the image data into the queue. However, Kemeny describes a first (42-0, Figure 3) and second (42-1) FIFO queue with different access frequencies. The second FIFO queue receives data from the first FIFO queue (Col. 10, line 59-Col. 11, line 7). Therefore, the second FIFO queue must inherently write the data into the queue on the first access frequency of the first FIFO queue, then output the data on the second access frequency of the second FIFO queue, so when running step(1) and step(2), both of them are working at the deferent frequency.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Marlton to include writing the image data into a queue as suggested by Kemeny because Kemeny suggests that the advantage of using FIFO queues is that data can be ordered according to priority (Col. 1, line 60-Col. 2, line 4).

14.   With regard to Claim 7, Marlton does not specifically teach that the second step First-In-First-Out (FIFO) unit has a one-input-one-output (FIFO) memory architecture implementing a transferring of the first and second access frequency. However, Min describes that the access frequency is determined by the FIFO capacity (Col. 1, lines 62-63). Marlton describes that the first step FIFO (550, Figure 5) has a capacity of 256Kx4 (Col. 10, lines 6-8) and the second step FIFO (224, Figure 13) has a capacity of 1 Mbit (Col. 14, lines 51-52). Since Marlton describes that the second step FIFO is receiving data that was in the first step FIFO and the FIFOs have different capacities, the second step FIFO must inherently receive image data at the first access frequency and output image data at the second access frequency, as discussed in the rejection for

Claim 1. Therefore, the second step FIFO has a one-input-one-output (FIFO) memory architecture implementing a transferring of the first and second access frequency.

15.   Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marlton (US005594467A), in view of Min (US006184907B1), further in view of Yamada (US006333788B1), further in view of Kemeny (US006701393B1), further in view of Welles (US004646151A).

Marlton, Min, Yamada, and Kemeny are relied upon for the teachings as discussed above relative to Claim 4. Marlton describes a method for an image reducing processing circuit (Col. 7, lines 33-35, 42-45; Col. 8, lines 9-11, 47-49, 56-59; Col. 25, lines 7-9) and a first step FIFO (500, Figure 5; Col. 10, lines 6-14).

However, Marlton, Min, Yamada, and Kemeny do not teach that the first step First-In-First-Out (FIFO) unit has the memory depth equal to a memory depth of the reduced image. However Welles describes a FIFO with a memory depth that can be expanded to any desired amount. Welles describes that the FIFO memory depth is sufficient for the image data (Col. 6, line 67-Col. 7, line 3; Col. 5, lines 7-10). Therefore, Welles inherently describes that the FIFO unit has the memory depth equal to a memory depth of the image.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Marlton, Min, Yamada, and Kemeny so that the first step First-In-First-Out (FIFO) unit has the memory depth equal to a memory depth of the reduced image as suggested by Welles because Welles suggests the advantage of having sufficient memory to store the image (Col. 6, line 67-Col. 7, line 3; Col. 5, lines 7-10).
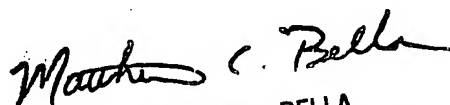
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 703-305-4418. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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